REMARKS

Claims 1-4 are all the claims pending in the application.

Claims 3 and 4 have been amended to address the claim objections and 35 U.S.C. § 112 rejections. These amendments are not intended to narrow the scope of the claims; therefore, no additional searching should be required. In addition, these amendments place the application in better condition for appeal by narrowing the outstanding issues. Therefore, the Examiner is requested to enter this after Final amendment.

Claim Objections

The Examiner objects to claims 3 and 4 as containing several informalities. The claims have been amended to address these objections. Therefore, the Examiner is requested to withdraw the objections.

35 U.S.C. § 112, First Paragraph Rejections

The Examiner objects to the language "logic operation delay information" in claims 3 and 4. Applicants have amended the claims to recite "logic operation information." Therefore, the Examiner is requested to withdraw the rejections.

35 U.S.C. § 112, Second Paragraph Rejection

The Examiner objects to the language "said at least one circuit" in claim 2. Applicants have amended the claims to recite "logic operation information." Therefore, the Examiner is requested to withdraw the rejections.

Prior Art Rejections

Regarding the prior art rejections, Applicants incorporate their comments from the November 16, 2006 Amendment. In addition, Applicants have the following additional comments.

In the claimed invention, the delay time is determined by comparing the input signal at a first point and the propagated signal (signal at a subsequent circuit point after propagation) at the second point. For example, assume that the data signal of a first flip-flop is "rising edge" at the first time point when a clock signal is input. Then, at the time point when the next clock signal is received, the question is whether or not the propagated signal at the next flip-flop is propagated as "rising edge" (in other words, whether the next trigger of the clock signal can occur in association with the rising edge of the propagated signal).

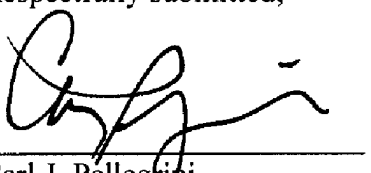
Figure 3, for example, represents the logical consequence of an AND gate (two inputs 1 and 2, and output 3) of figure 2. Assume the case where the state changes LOW-HIGH-LOW within a period of two clock signals. At the time in which the second clock signal is input, the state is "LOW," which is regarded to be the same state as the first signal state. Thus, there is no recognition of "rising" (LOW-HIGH) in view of the operation per clock unit. Therefore, the case where the delay is "NONE" (at the column Rise/Fall), will not indicate any change in the signal state (between LOW and HIGH) which means that there is no need to make a target (object) of the timing analysis for the case "NONE" in figure 3. In the claimed invention, the situation where there is no change in signal state (i.e., a nullified state) is determined automatically as a result of the logic AND circuit. See specification at page 5, line 2 through page 6, line 11.

On the other hand, in Hasegawa '511, the occurrence of a "nullified state" must be identified explicitly.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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